Abstract of the Disclosure

The present invention provides a semiconductor memory device. In the semiconductor device, third and fourth transistors are configured as a vertical structure. The third transistor is laminated over a first transistor, and the fourth transistor is laminated over a second transistor, whereby a reduction in cell area is achieved. A voltage set on the condition that the difference between a source potential applied to each of the first and second transistors and the potential of a select level of a word line becomes greater than or equal to a threshold voltage of each of the third and fourth transistors, is supplied to a source electrode of each of the first and second transistors to thereby perform "0" write compensation.